WHAT IS CLAIMED IS:

1. A method of integrating a plurality of subcircuit grids in a simulation environment, comprising:

obtaining a subcircuit layer of a particular granularity for each logical component of an electrical entity under simulation; and

interconnecting nodes of a first subcircuit layer to nodes of a second subcircuit layer using a constraint-based search process.

2. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 1, wherein said electrical entity under simulation comprises a semiconductor die disposed in a package and board environment.

3. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 2, wherein said subcircuit layer comprises an on-chip power grid subcircuit layer.

4. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 2, wherein said subcircuit layer comprises an on-chip load subcircuit layer.

5. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 2, wherein said subcircuit layer comprises a package-level subcircuit layer.

6. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 2, wherein said subcircuit layer comprises a die-level subcircuit layer.

7. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 2, wherein said subcircuit layer comprises a board-level subcircuit layer.

8. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 1, wherein said first and second subcircuit layers are disposed adjacent to each other.

9. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 1, wherein said search process is operable to interconnect a node (N1) of said first subcircuit layer to a node (N2) of said second subcircuit layer based on minimizing a distance between said N1 and N2 nodes.

10. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 9, wherein said search process is operable to determine if said second subcircuit layer contains any nodes within a first search region defined with respect to a point that corresponds to said N1 node's coordinates.

11. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 10, wherein said search process is operable to provide an error indication if said second subcircuit layer does not include any nodes within said first search region.

12. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 10, wherein said search process is operable to expand said first search region to a second search region if said second subcircuit layer does not include any nodes within said first search region.

13. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 12, wherein said search process is operable to provide an error indication if said second subcircuit layer does not include any nodes within said second search region.

14. The method of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 1, wherein a node (N1) of said first subcircuit layer is interconnected to a node (N2) of said second subcircuit layer by a connector subcircuit disposed therebetween.

15. A system for integrating a plurality of subcircuit grids in a simulation environment, comprising:

means for obtaining a subcircuit layer of a particular granularity for each logical component of an electrical entity under simulation; and

means for interconnecting nodes of a first subcircuit layer to nodes of a second subcircuit layer using a constraint-based search process.

16. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 15, wherein said electrical entity under simulation comprises a semiconductor die disposed in a package and board environment.

17. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 16, wherein said subcircuit layer comprises an on-chip power grid subcircuit layer.

18. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 16, wherein said subcircuit layer comprises an on-chip load subcircuit layer.

19. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 16, wherein said subcircuit layer comprises a package-level subcircuit layer.

20. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 16, wherein said subcircuit layer comprises a die-level subcircuit layer.

21. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 16, wherein said subcircuit layer comprises a board-level subcircuit layer.

22. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 15, wherein said first and second subcircuit layers are disposed adjacent to each other.

23. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 15, wherein said search process is operable to interconnect a node (N1) of said first subcircuit layer to a node (N2) of said second subcircuit layer based on minimizing a distance between said N1 and N2 nodes.

24. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 23, wherein said search process is operable to determine if said second subcircuit layer contains any nodes within a first search region defined with respect to a point that corresponds to said N1 node's coordinates.

25. The system of integrating a plurality of subcircuit grids in a simulation environment as recited in claim 24, wherein said search process is operable to provide an error indication if said second subcircuit layer does not include any nodes within said first search region.

26. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 24, wherein said search process is operable to expand said first search region to a second search region if said second subcircuit layer does not include any nodes within said first search region.

27. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 26, wherein said search process is operable to provide an error indication if said second subcircuit layer does not include any nodes within said second search region.

28. The system for integrating a plurality of subcircuit grids in a simulation environment as recited in claim 15, wherein a node (N1) of said first subcircuit layer is interconnected to a node (N2) of said second subcircuit layer by a connector subcircuit disposed therebetween.

29. A computer-accessible medium operable with a computer platform to support a design simulation environment, the medium having stored thereon instructions for integrating a plurality of subcircuit grids generated in said design simulation environment, comprising:

program code for obtaining a subcircuit layer of a particular granularity for each logical component associated with an electrical entity under simulation; and

program code for interconnecting nodes of a first subcircuit layer to nodes of a second subcircuit layer using a constraint-based search process.

30. The computer-accessible medium as recited in claim 29, wherein said electrical entity under simulation comprises a semiconductor die disposed in a package and board environment.

31. The computer-accessible medium as recited in claim 30, wherein said subcircuit layer comprises an on-chip power grid subcircuit layer.

32. The computer-accessible medium as recited in claim 30, wherein said subcircuit layer comprises an on-chip load subcircuit layer.

33. The computer-accessible medium as recited in claim 30, wherein said subcircuit layer comprises a package-level subcircuit layer.

34. The computer-accessible medium as recited in claim 30, wherein said subcircuit layer comprises a die-level subcircuit layer.

35. The computer-accessible medium as recited in claim 30, wherein said subcircuit layer comprises a board-level subcircuit layer.

36. The computer-accessible medium as recited in claim 29, wherein said first and second subcircuit layers are disposed adjacent to each other.

37. The computer-accessible medium as recited in claim 29, wherein said search process is operable to interconnect a node (N1) of said first subcircuit layer to a node (N2) of said second subcircuit layer based on minimizing a distance between said N1 and N2 nodes.

38. The computer-accessible medium as recited in claim 37, wherein said search process is operable to determine if said second subcircuit layer contains any nodes within a first search region from a point that corresponds to said N1 node's coordinates.

39. The computer-accessible medium as recited in claim 38, wherein said search process is operable to provide an error indication if said second subcircuit layer does not include any nodes within said first search region.

40. The computer-accessible medium as recited in claim 38, wherein said search process is operable to expand said first search region to a second search region if said second subcircuit layer does not include any nodes within said first search region.

41. The computer-accessible medium as recited in claim 40, wherein said search process is operable to provide an error indication if said second subcircuit layer does not include any nodes within said second search region.

42. The computer-accessible medium as recited in claim 29, wherein a node (N1) of said first subcircuit layer is interconnected to a node (N2) of said second subcircuit layer by a connector subcircuit disposed therebetween.